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EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/753,764	Applicant(s) KOTTAPALLI, SAILESH
	Examiner David J. Huisman	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 April 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 4/18/2005.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Due to the amendments made to the claims during prosecution, the title should now be amended to more accurately reflect the content of the claims.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: In Fig.2, the examiner has been unable to find reference numbers 212, 214, 216, 234, 236, 238, 240, 242, and 244 within the specification. In Fig.3, the examiner has been unable to find reference numbers 302, 308, 310, 312, 314, 316, 334, 336, 338, 340, 342, and 344 within the specification. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

6. Claims 1-4, 9-13, and 18-21 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art (herein referred to as AAPA).

7. Referring to claim 1, AAPA has taught a simultaneous multithreaded processor system comprising:

a) a first multiplexer associated with instruction pointers of a first thread. See Fig.2, component 218.

b) a second multiplexer associated with instruction pointers of a second thread. See Fig.2, component 220.

c) a first storage element dedicated to the first multiplexer. See Fig.2, component 248, for instance, and note that the storage element is dedicated to holding inactive thread pointers from the first multiplexer. The American Heritage® Dictionary of the English Language defines "dedicate" as "to set apart for a special use" (see attached definition). Clearly, when the first multiplexer is associated with the inactive thread, then storage element 248 is dedicated only to holding pointers from that multiplexer (i.e., it is set aside for special use by the first multiplexer).

d) a second storage element dedicated to the second multiplexer. See Fig.2, component 250, for instance, and note that the storage element is dedicated to holding inactive thread pointers from the second multiplexer. The American Heritage® Dictionary of the English Language defines "dedicate" as "to set apart for a special use" (see attached definition). Clearly, when the second

multiplexer is associated with the inactive thread, then storage element 250 is dedicated only to holding pointers from that multiplexer (i.e., it is set aside for special use by the second multiplexer).

e) said first and second multiplexers to provide said instruction pointers of said first and second threads for execution in said processor. See Fig.2 and note that MUXs 218 and 220 provide pointers to subsequent stages in the pipeline (which includes an execution stage 212).

f) one of the first and second threads is to be active while the other of said first and second threads is inactive. Note that MUX 246 only has one output. This will be either an instruction from a first thread or an instruction from a second thread. The thread that is selected will be active; the other will be inactive.

g) said instruction pointers for the active thread are to be delivered to processor logic. If the first thread is active, then the output of MUX 218 will be selected for output by MUX 246 and proceed to processor logic in additional pipeline stages. Likewise, if the second thread is active, then the output of MUX 220 will be selected for output by MUX 246 and proceed to processor logic in additional pipeline stages.

h) if the first thread is inactive, said instruction pointers for the first thread are to be delivered to the first storage element for delivery to the processor logic if the first thread becomes active. As disclosed on page 2, lines 21-23, of applicant's background, the storage elements are used to store instruction pointers for the inactive thread (in this case, the first thread). That is, if the first thread is inactive, instruction pointers from the first multiplexer will be re-steered (via re-steer logic) to the first storage element (which could also include storage element 252, for instance).

The first storage element is then able to provide these instruction pointers to the MUX 220, which would output the instructions to processor logic when the first thread becomes active.

i) if the second thread is inactive, said instruction pointers for the second thread are to be delivered to the second storage element for delivery to the processor logic if the second thread becomes active. As disclosed on page 2, lines 21-23, of applicant's background, the storage elements are used to store instruction pointers for the inactive thread (in this case, the second thread). That is, if the second thread is inactive, instruction pointers from the second multiplexer will be re-steered (via re-steer logic) to the second storage element (which could also include storage element 254, for instance). The second storage element is then able to provide these instruction pointers to the MUX 220, which would output the instructions to processor logic when the second thread becomes active.

8. Referring to claim 2, AAPA has taught a system as described in claim 1. AAPA has further taught a common multiplexer coupled between said first and second multiplexer and processor logic. See Fig.2, component 246.

9. Referring to claim 3, AAPA has taught a system as described in claim 2. AAPA has further taught that the common multiplexer is to receive instruction pointer data sequentially from the first multiplexer and the second multiplexer by utilizing a time-multiplexing protocol. See page 2, lines 17-19, of applicant's specification (background information section).

10. Referring to claim 4, AAPA has taught a system as described in claim 3. AAPA has further taught that the time-multiplexing protocol is a `round-robin` protocol. See page 2, lines 17-19, of applicant's specification (background information section).

11. Referring to claim 9, AAPA has taught a system as described in claim 1. AAPA has further taught that the storage element is a flip-flop device. See page 2, line 21.

12. Referring to claim 10, AAPA has taught a method for a simultaneous multithreaded processor system, comprising the steps of:

a) associating a first multiplexer with instruction pointers of a first thread. See Fig.2, component 218.

b) associating a second multiplexer with instruction pointers of a second thread. See Fig.2, component 220.

c) providing, by said first and second multiplexers, said instruction pointers of said first and second threads for execution in said processor. See Fig.2 and note that MUXs 218 and 220 provide pointers to subsequent stages in the pipeline (which includes an execution stage 212).

d) dedicating a first storage element to the first multiplexer. . See Fig.2, component 248, for instance, and note that the storage element is dedicated to holding inactive thread pointers from the first multiplexer. The American Heritage® Dictionary of the English Language defines "dedicate" as "to set apart for a special use" (see attached definition). Clearly, when the first multiplexer is associated with the inactive thread, then storage element 248 is dedicated only to holding pointers from that multiplexer (i.e., it is set aside for special use by the first multiplexer).

e) dedicating a second storage element to the second multiplexer. See Fig.2, component 250, for instance, and note that the storage element is dedicated to holding inactive thread pointers from the second multiplexer. The American Heritage® Dictionary of the English Language defines "dedicate" as "to set apart for a special use" (see attached definition). Clearly, when the second multiplexer is associated with the inactive thread, then storage element 250 is dedicated only to

holding pointers from that multiplexer (i.e., it is set aside for special use by the second multiplexer).

f) establishing one of the first and second threads as active and the other of said first and second threads as inactive. Note that MUX 246 only has one output. This will be either an instruction from a first thread or an instruction from a second thread. The thread that is selected will be active; the other will be inactive.

g) delivering said instruction pointers for the active thread to processor logic. If the first thread is active, then the output of MUX 218 will be selected for output by MUX 246 and proceed to processor logic in additional pipeline stages. Likewise, if the second thread is active, then the output of MUX 220 will be selected for output by MUX 246 and proceed to processor logic in additional pipeline stages.

h) if the first thread is inactive, delivering said instruction pointers for the first thread to the first storage element for delivery to the processor logic if the first thread becomes active. As disclosed on page 2, lines 21-23, of applicant's background, the storage elements are used to store instruction pointers for the inactive thread (in this case, the first thread). That is, if the first thread is inactive, instruction pointers from the first multiplexer will be re-steered (via re-steer logic) to the first storage element (which could also include storage element 252, for instance). The first storage element is then able to provide these instruction pointers to the MUX 220, which would output the instructions to processor logic when the first thread becomes active.

i) if the second thread is inactive, delivering said instruction pointers for the second thread to the second storage element for delivery to the processor logic if the second thread becomes active. As disclosed on page 2, lines 21-23, of applicant's background, the storage elements are used to

store instruction pointers for the inactive thread (in this case, the second thread). That is, if the second thread is inactive, instruction pointers from the second multiplexer will be re-steered (via re-steer logic) to the second storage element (which could also include storage element 254, for instance). The second storage element is then able to provide these instruction pointers to the MUX 220, which would output the instructions to processor logic when the second thread becomes active.

13. Referring to claim 11, AAPA has taught a method as described in claim 10. Furthermore, the system of claim 2 performs the method of claim 11. Therefore, claim 11 is rejected for the same reasons set forth in the rejection of claim 2 above.

14. Referring to claim 12, AAPA has taught a method as described in claim 11. Furthermore, the system of claim 3 performs the method of claim 12. Therefore, claim 12 is rejected for the same reasons set forth in the rejection of claim 3 above.

15. Referring to claim 13, AAPA has taught a method as described in claim 12. Furthermore, the system of claim 4 performs the method of claim 13. Therefore, claim 13 is rejected for the same reasons set forth in the rejection of claim 4 above.

16. Referring to claim 18, AAPA has taught a method as described in claim 10. Furthermore, the system of claim 9 performs the method of claim 18. Therefore, claim 18 is rejected for the same reasons set forth in the rejection of claim 9 above.

17. Referring to claim 19, AAPA has taught a simultaneous multithreaded processor system comprising:

a) a first multiplexer associated with instruction pointers of a first thread. See Fig.2, component 218.

b) a second multiplexer associated with instruction pointers of a second thread. See Fig.2, component 220.

c) a first storage element dedicated to the first multiplexer.

d) a second storage element dedicated to the second multiplexer.

e) said first and second multiplexers provide said instruction pointers of said first and second threads for execution in said processor. See Fig.2 and note that MUXs 218 and 220 provide pointers to subsequent stages in the pipeline (which includes an execution stage 212).

f) one of the first and second threads is to be active while the other of said first and second threads is inactive. Note that MUX 246 only has one output. This will be either an instruction from a first thread or an instruction from a second thread. The thread that is selected will be active; the other will be inactive.

g) said instruction pointers for the active thread are delivered to processor logic. If the first thread is active, then the output of MUX 218 will be selected for output by MUX 246 and proceed to processor logic in additional pipeline stages. Likewise, if the second thread is active, then the output of MUX 220 will be selected for output by MUX 246 and proceed to processor logic in additional pipeline stages.

h) if the first thread is inactive, said instruction pointers for the first thread are to be delivered to the first storage element for delivery to the processor logic if the first thread becomes active. As disclosed on page 2, lines 21-23, of applicant's background, the storage elements are used to store instruction pointers for the inactive thread (in this case, the first thread). That is, if the first thread is inactive, instruction pointers from the first multiplexer will be re-steered (via re-steer logic) to the first storage element (which could also include storage element 252, for instance).

The first storage element is then able to provide these instruction pointers to the MUX 220, which would output the instructions to processor logic when the first thread becomes active.

i) if the second thread is inactive, said instruction pointers for the second thread are to be delivered to the second storage element for delivery to the processor logic if the second thread becomes active. As disclosed on page 2, lines 21-23, of applicant's background, the storage elements are used to store instruction pointers for the inactive thread (in this case, the second thread). That is, if the second thread is inactive, instruction pointers from the second multiplexer will be re-steered (via re-steer logic) to the second storage element (which could also include storage element 254, for instance). The second storage element is then able to provide these instruction pointers to the MUX 220, which would output the instructions to processor logic when the second thread becomes active.

j) a common multiplexer coupled between said first and second multiplexer and processor logic that is to receive instruction pointer data sequentially from the first multiplexer and the second multiplexer by utilizing a time-multiplexing protocol. See Fig.2, component 246, and see page 2, lines 17-19, of applicant's specification (background information section).

18. Referring to claim 20, AAPA has taught a system as described in claim 19. AAPA has further taught that the first multiplexer and the second multiplexer are to receive instruction pointer information and data from a plurality of stages in a processor pipeline. See Fig.2, and note that MUXs 218 and 220 receive pointer information and data from various pipeline stages, including the IPG-1, IPG+1, IPG+2, and CMT stages.

19. Referring to claim 21, AAPA has taught a system as described in claim 20. AAPA has further taught that the first multiplexer and the second multiplexer are to receive instruction

pointer information and data from re-steer logic at the plurality of stages in the processor pipeline. See Fig.2, and note that the information is received from re-steer logic located in a plurality of pipeline stages (the re-steer logic includes the boxes labeled 1-6).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 5-8, 14-17, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, as applied above.

22. Referring to claim 5, AAPA has taught a system as described in claim 1. Although AAPA's Fig.2 utilizes time-multiplexing between two threads (page 2, lines 17-19), AAPA has not explicitly taught that the first multiplexer and the second multiplexer are priority multiplexers. However, AAPA also shows that priority multiplexers are known in the art. See Fig.1. In addition, from page 2, lines 6-9 of applicant's specification, it has been taught that a thread may be switched if a higher priority thread needs attention. As a result, it would have been obvious to one of ordinary skill in the art to modify the first and second multiplexers of Fig.2 to be priority multiplexers so that more important threads, having highest priority, are executed as soon as possible.

23. Referring to claim 6, AAPA has taught a system as described in claim 5. AAPA has further taught that the first multiplexer and the second multiplexer are to receive instruction

pointer information and data from a plurality of stages in a processor pipeline. See Fig.2, and note that MUXs 218 and 220 receive pointer information and data from various pipeline stages, including the IPG-1, IPG+1, IPG+2, and CMT stages.

24. Referring to claim 7, AAPA has taught a system as described in claim 6. AAPA has further taught that the first multiplexer and the second multiplexer receive instruction pointer information and data from re-steer logic at the plurality of stages in the processor pipeline. See Fig.2, and note that the information is received from re-steer logic located in a plurality of pipeline stages (the re-steer logic includes the boxes labeled 1-6).

25. Referring to claim 8, AAPA has taught a system as described in claim 7. AAPA has not explicitly taught that the first and second multiplexers (of Fig.2) are to pass the instruction pointer information and data to the common multiplexer with a pre-determined priority. However, AAPA has taught the concept of a multiplexer which passes instruction pointer information and data with a pre-determined priority. See Fig.1, and page 4, line 16, to page 5, line 9, of applicant's specification. Such a multiplexer allows for switching threads such that the highest priority thread receives immediate attention. See page 2, lines 6-9 of applicant's specification. As a result, it would have been obvious to one of ordinary skill in the art to modify Fig.2 of AAPA such that the first and second multiplexers (of Fig.2) pass the instruction pointer information and data to the common multiplexer with a pre-determined priority so that more important threads, having highest priority, are executed as soon as possible.

26. Referring to claim 14, AAPA has taught a method as described in claim 10. Furthermore, the system of claim 5 performs the method of claim 14. Therefore, claim 14 is rejected for the same reasons set forth in the rejection of claim 5 above.

27. Referring to claim 15, AAPA has taught a method as described in claim 14. Furthermore, the system of claim 6 performs the method of claim 15. Therefore, claim 15 is rejected for the same reasons set forth in the rejection of claim 6 above.

28. Referring to claim 16, AAPA has taught a method as described in claim 15. Furthermore, the system of claim 7 performs the method of claim 16. Therefore, claim 16 is rejected for the same reasons set forth in the rejection of claim 7 above.

29. Referring to claim 17, AAPA has taught a method as described in claim 16. Furthermore, the system of claim 8 performs the method of claim 17. Therefore, claim 17 is rejected for the same reasons set forth in the rejection of claim 8 above.

30. Referring to claim 22, AAPA has taught a system as described in claim 19. AAPA has not explicitly taught that the first and second multiplexers (of Fig.2) pass the instruction pointer information and data to the common multiplexer with a pre-determined priority. However, AAPA has taught the concept of a multiplexer which passes instruction pointer information and data with a pre-determined priority. See Fig.1, and page 4, line 16, to page 5, line 9, of applicant's specification. Such a multiplexer allows for switching threads such that the highest priority thread receives immediate attention. See page 2, lines 6-9 of applicant's specification. As a result, it would have been obvious to one of ordinary skill in the art to modify Fig.2 of AAPA such that the first and second multiplexers (of Fig.2) pass the instruction pointer information and data to the common multiplexer with a pre-determined priority so that more important threads, having highest priority, are executed as soon as possible.

Response to Arguments

31. Applicant's arguments filed on April 18, 2005, have been fully considered but they are not persuasive.

32. Applicant argues the novelty/rejection of claims 1, 10, and 19 on pages 11-12 of the remarks. More specifically, applicant argues that the examiner provided the definition for "dedicate" and not "dedicated," and that according to applicant's cited dictionary, "dedicated" is defined as "intended for only one purpose: designed to carry out only one task, or set aside for a purpose." Applicant further argues that based on this definition, storage element 248 of AAPA is not dedicated to multiplexer 218 or 220 because it receives data from both of them (therefore, it is a shared element and not a dedicated element).

33. These arguments are not found persuasive for the following reasons:

a) Even when taking applicant's definition of "dedicated" into consideration, AAPA still anticipates the claimed subject matter. AAPA is involved with multiple threads, wherein threads are switched from active to inactive and vice-versa. As discussed in the rejection of the independent claims, storage element 248 is dedicated to the first multiplexer when the first multiplexer is associated with the inactive thread, and storage element 250 is dedicated to the second multiplexer when the second multiplexer is associated with the inactive thread. The examiner agrees with applicant that the storage elements may receive data from both multiplexers, but this is only true when tracking system operation as a whole (from start to end times). When looking at certain windows of time, however, it should be realized that these storage elements are dedicated to their respective multiplexers.

For instance, assume at time T0, a first thread associated with the first multiplexer is active while a second thread associated with the second multiplexer is inactive. Then, at time

T4, the first thread associated with the first multiplexer is switched to inactive while the second thread associated with the second multiplexer is switched to active. Finally, at T8, the first thread associated with the first multiplexer is switched to active while the second thread associated with the second multiplexer is switched to inactive. As is known from AAPA, when a thread is active, its multiplexer outputs instructions that are to propagate through the pipeline for execution. When a thread is inactive, its multiplexer outputs instructions that are re-steered to storage elements, so that when the thread becomes active at some point in the future, the instructions may be reintroduced into the system. Looking at individual time windows, the following can be realized:

T4-T7: storage element 248 accepts inactive instruction pointers associated with the first thread and first multiplexer. During this time, element 248 does not accept pointers from the second multiplexer. Hence, element 248, during the T4-T7 time range, is dedicated to the first multiplexer, i.e., it is intended for only one purpose (to hold inactive thread instructions associated with the first multiplexer).

T8-TX: storage element 250 accepts inactive instruction pointers associated with the second thread and second multiplexer. During this time, element 250 does not accept pointers from the first multiplexer. Hence, element 250, during the T8-TX time range (TX being the time when the next thread switch occurs), is dedicated to the second multiplexer, i.e., it is intended for only one purpose (to hold inactive thread instructions associated with the second multiplexer).

The examiner believes that this is a sufficient interpretation of "dedicated" and that the interpretation is not inconsistent with the way "dedicated" is used in the art, as it is not 100% clear to the examiner how "dedicated" is used in the art. Unlike the words "CPU" and "RAM"

(which are well known words that have well known meanings in the art), the word "dedicated" is not so cut-and-dry. Even if an example exists which shows "dedicated" to mean complete dedication at all times, can applicant conclude that "dedicated" is always used in this manner, based on one example? For instance, in a thread switching system, in which one thread executes at a time, is the system hardware not dedicated to executing the active thread? When another thread becomes active, is the hardware not dedicated to executing the new active thread? Or, can a person not be dedicated to studying hard for a math class and dedicated to studying hard for a history class at the same time? Applicant's claim says nothing about the storage elements being dedicated to only one multiplexer at all times throughout the course of system operation (i.e., applicant never rules out that a storage element cannot receive pointers from a non-associated multiplexer). As the examiner has shown, if you take an individual time window and analyze the operation of the system within that time window, storage element dedication is clear. Looking at the system as a whole (from T0-T∞), complete dedication is not taught by AAPA, but this does not change the fact that AAPA does teach complete dedication during individually time windows. And, it is the operation within these time windows which read on applicant's claims.

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
May 5, 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100